

What is claimed is:

1. A multi-phase-locked loop for data recovery comprising a phase detector, a charge pump, a loop filter and a voltage controlled oscillator, wherein:
- said phase detector is constituted by N phase detection units (U_1, U_2, \dots, U_N , N is even, $N \geq 4$); said N phase detection units are connected in cascade configuration, and each phase detection unit contains a data signal input terminal for receiving a data signal from outside; a clock signal input terminal for receiving the multi-phase clock signals (CK_1, CK_2, \dots, CK_N) from outside; a delay signal input terminal for receiving a delay signal output from another phase detection unit; a delay signal output terminal for outputting a delay signal; and a charge/discharge control signal output terminal for outputting control signals for charge/discharge operations; each of said N phase detection units generates a delay signal (D_1, D_2, \dots, D_N) according to an input data signal and the complement of a multi-phase clock signal; the delay signal (D_{j+1}) generated by the $(j+1)_{th}$ phase detection unit is input into the j_{th} phase detection unit via the j_{th} delay signal input terminal; the delay signal (D_1) generated by the first phase detection unit is input into the N_{th} phase detection unit via the N_{th} delay signal input terminal; the j_{th} phase detection unit (U_j , $1 \leq j < N$, j is a positive integer) generates control signals ($dn_1, dn_2, \dots, dn_{N/2}, up_{N/2}, \dots, up_2$) for charge/discharge operations according to the delay signal (D_j) from the j_{th} phase detection unit, the

delay signal (D_{j+1}) from the $(j+1)_{th}$ phase detection unit,
and the multi-phase clock signal (CK_j) which is applied
to the j_{th} phase detection unit; the N_{th} phase detection
unit generates a charge control signal (up_1) according
5 to the delay signal (D_n) from the N_{th} phase detection unit,
the delay signal (D_1) from the first phase detection unit,
and the multi-phase clock signal (CK_N) which is applied
to the N_{th} phase detection unit;

said charge pump being constituted by $N/2$ charge and
10 discharge units ($CP_1, CP_2, \dots, CP_{N/2}$), wherein the k_{th} (CP_k ,
 $1 \leq k \leq N/2$) charge and discharge unit (CP_k) is employed to
receive the k_{th} charge/discharge control signal set
(up_k/dn_k) from said phase detector, and a current I_{ch_k} is
generated by the charge/discharge control signal set
15 (up_k/dn_k); the charge/discharge current $I_{ch_k} = (w_k \times up_k -$
 $w_k \times dn_k) I_{ss}$, wherein w_k is a weighting value, I_{ss} is a fixed
current value, and $w_1 < w_2 < \dots < w_{N/2}$; the total
charge/discharge current (I_{ch}) from said charge pump
equals to $I_{ch_1} + I_{ch_2} + \dots + I_{ch_k} + \dots + I_{ch_{N/2}}$; and said
20 voltage controlled oscillator is a multi-phase voltage
controlled oscillator, which outputs N multi-phase clock
signals (CK_1, CK_2, \dots, CK_N), which are applied to said phase
detectors, respectively.

2. The multi-phase-locked loop for data recovery as
25 described in claim 1, wherein the phase difference
between the multi-phase clock signal (CK_{j+1}) input to the
 $(j+1)_{th}$ phase detection unit (U_{j+1}) and the multi-phase
clock signal (CK_j) input to the j_{th} phase detection unit
(U_j) equals to $2\pi/N$.

30 3. The multi-phase-locked loop for data recovery as

described in claim 1, wherein each of said N phase detection unit comprises: an inverter, a first flip-flop, an exclusive OR gate, and a second flip-flop;

5 said inverter inverting multi-phase clock signal which is to be input to each phase detection unit; the first flip-flop generating a delay signal according to the complementary multi-phase clock signal from said inverter and the data signal; the delay signal from said first flip-flop and the delay signal from the first
10 flip-flop in another phase detection unit being input to the exclusive OR gate; the second flip-flop generating a charge/discharge control signal according to the multi-phase clock signal and the output signal from said exclusive OR gate.

15 4. The multi-phase-locked loop for data recovery as
described in claim ~~2~~³, wherein said first flip-flop and
said second flip-flop are D flip-flops.